Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	165	(phase adj (changeable)) and semiconductor	US-PGPUB; USPAT	OR	ON	2005/02/09 11:06
L2	118	1 and @ad<"20021101"	US-PGPUB; USPAT	OR	ON	2005/02/09 11:07
L3	14	(phase adj (changeable)) and semiconductor	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/09 11:05
L4	8391	(phase adj (change)) and semiconductor	US-PGPUB; USPAT	OR	ON	2005/02/09 11:06
L5	1251	(phase adj (change) adj material) and semiconductor	US-PGPUB; USPAT	OR	ON	2005/02/09 11:17
L6	841	5 and @ad<"20021101"	US-PGPUB; USPAT	OR	ON	2005/02/09 11:07
L7	799	6 not 2	US-PGPUB; USPAT	OR	ON	2005/02/09 11:07
L8	36	(phase adj (change) adj material) and semiconductor	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/09 11:18

US-PAT-NO: 6764894

DOCUMENT-IDENTIFIER: US 6764894 B2

TITLE: Elevated pore phase-change memory

--------- KWIC ---------

Brief Summary Text - BSTX (2):
This invention relates generally to memories that use **phase-change materials**.

Brief Summary Text - BSTX (3):
Phase-change materials may exhibit at least two different states. The states may be called the amorphous and crystalline states. Transitions between these states may be selectively initiated in response to temperature changes. The states may be distinguished because the amorphous state generally exhibits higher resistivity than the crystalline state. The amorphous state involves a more disordered atomic structure and the crystalline state involves a more ordered atomic structure. Generally, any **phase-change material** may be utilized. In some embodiments, however, thin-film chalcogenide alloy materials may be particularly suitable.

Brief Summary Text - BSTX (7):
A **phase-change material** may be formed within a passage or pore defined through a dielectric material. The **phase-change material** may be coupled to contacts on either end of the passage. State transitions may be induced by applying a current to heat the **phase-change material**.

Brief Summary Text - BSTX (8):
An access device may be defined in the substrate of a semiconductor integrated circuit to activate an overlying **phase-change material**. Other phase-change memory components may also be integrated into the semiconductor substrate. Patterning features over integrated topography may adversely impact the underlying integrated features. Thus, it would be desirable to form the phase-change memory in a fashion, above the rest of the integrated circuit, that does not interfere with any of the previously fabricated integrated structures.

Brief Summary Text - BSTX (9):
Another issue with phase-change memories is that the greater the heat loss from each memory cell, the greater the current that must be applied for device programming. Thus, it would be desirable to reduce the amount of heat loss from the heated **phase-change material**. Similarly, it is desirable to distribute the heat homogenously across the **phase-change material**. However, many currently proposed techniques result in local variations in device resistance after a programming event. These local variations may also result

in stress in local regions during the phase-change programming.

Detailed Description Text - DETX (3):
The elevated pore includes a resistive or lower electrode 22 that may also be tubular and cup-shaped. Within the interior of the lower electrode 22 is a pore defined by a pair of opposed spacers 24 and a phase-change layer 28. The phase-change layer 28 also may be cup-shaped and may be filled with an upper electrode 30 in one embodiment of the present invention. The upper electrode 30 and the **phase-change material** 28 may be patterned in one embodiment of the present invention.

Detailed Description Text - DETX (11):
Then, as shown in FIG. 2I, the structure shown in FIG. 2H may be covered by a phase-change layer 28 and an upper electrode layer 30. In one embodiment, the phase-change layer 28 is cup-shaped and extends downwardly into the pore defined by the spacer 24 on the sides and the lower electrode 22 on the bottom. In one embodiment, the **phase-change material** may be Ge.sub.2 Sb.sub.2 Te.sub.5.

Claims Text - CLTX (1):
1. A method comprising: forming a base contact in a semiconductor structure; covering said semiconductor structure with a layer; forming a tubular electrical connection through said layer to said contact; depositing an insulator within said electrical connection; and forming a cup-shaped heater electrically coupled to said tubular electrical connection; and forming a **phase-change material** over said layer, said material electrically coupled to said contact through said connection and said cup-shaped heater.

Claims Text - CLTX (6):
6. The method of claim 5 wherein forming a **phase-change material** includes depositing a **phase-change material** over said insulating layer and said spacer and electrically contacting said lower electrode.

Claims Text - CLTX (7):
7. A method comprising: forming a base contact in a semiconductor structure; covering said semiconductor structure with a layer; forming a first cup-shaped electrical connection through said layer to said contact; forming a second cup-shaped connection layer over said first cup-shaped connection layer and an electrical communication therewith; forming a **phase-change material** over said second cup-shaped electrical connection layer, said **phase-change material** electrically coupled to said base contact by said first and second cup-shaped electrical connection layers; and filling said first cup-shaped electrical connection with an insulator.

Claims Text - CLTX (9):
9. The method of claim 8 including forming a **phase change material** by depositing a **phase-change material** over said layer and said spacer.

US-PAT-NO: 6566700

DOCUMENT-IDENTIFIER: US 6566700 B2

TITLE: Carbon-containing interfacial layer for phase-change memory

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Abstract Text - ABTX (1):
A phase-change memory cell may be formed with a carbon-containing interfacial layer that heats a **phase-change material**. By forming the **phase-change material** in contact, in one embodiment, with the carbon containing interfacial layer, the amount of heat that may be applied to the **phase-change material,** at a given current and temperature, may be increased. In some embodiments, the performance of the interfacial layer at high temperatures may be improved by using a wide band gap semiconductor material such as silicon carbide.

Brief Summary Text - BSTX (2):
This invention relates generally to memories that use **phase-change materials**.

Brief Summary Text - BSTX (3):
Phase-change materials may exhibit at least two different states. The states may be called the amorphous and crystalline states. Transitions between these states may be selectively initiated. The states may be distinguished because the amorphous state generally exhibits higher resistivity than the crystalline state. The amorphous state involves a more disordered atomic structure and the crystalline state involves a more ordered atomic structure. Generally, any **phase-change material** may be utilized; however, in some embodiments, thin-film chalcogenide alloy materials may be particularly suitable.

Brief Summary Text - BSTX (7):
A **phase-change material** may be formed within a passage or pore defined through a dielectric material. The **phase-change material** may be coupled to contacts on either end of the passage.

Brief Summary Text - BSTX (8):
The phase-change may be induced by heating the **phase-change material**. In some embodiments of phase-change memories, a current is applied through a lower electrode that has sufficient resistivity or other characteristics to heat the **phase-change material** and to induce the appropriate phase change. In some embodiments, the lower electrode may produce temperatures on the order of 600.degree. C.

Brief Summary Text - BSTX (10):

Thus, there is a need for a controllable way to provide sufficient resistance proximate to the **phase-change material** even at elevated temperatures.

Detailed Description Text - DETX (2):

Referring to FIG. 1, a memory cell 10 may include a **phase-change material** layer 24. The **phase-change material** layer 24 may be sandwiched between an upper electrode 26 and a lower electrode 14. In one embodiment, the lower electrode 14 may be cobalt silicide. However, the lower electrode 14 may be any conductive material. Similarly, the upper electrode 26 may be any conductive material.

Detailed Description Text - DETX (3):

The lower electrode 14 may be defined over a semiconductor substrate 12. Over the lower electrode 14, outside the region including the **phase-change material** layer 24, may be an insulative material 16, such as silicon dioxide or silicon nitride, as two examples. A buried wordline (not shown) in the substrate 12 may apply signals and current to the **phase-change material** 24 through the lower electrode 14.

Detailed Description Text - DETX (4):

A carbon-containing interfacial layer 20 may be positioned between the **phase-change material** layer 24 and the insulator 16. In one embodiment, a cylindrical sidewall spacer 22 may be defined within a tubular pore that is covered by the carbon-containing interfacial layer 20 and the **phase-change material** layer 24.

Detailed Description Text - DETX (5):

In one embodiment of the present invention, the carbon-containing interfacial layer 20 may be formed of silicon carbide. Silicon carbide, in its single crystal form, is a wide band gap semiconductor with alternating hexagonal planes of silicon and carbon atoms. Silicon carbide may be heated to 600.degree. C. in operation and may have a resistivity that does not significantly go down with increasing temperature. Therefore, silicon carbide is very effective for heating the **phase-change material** layer 24. Again, it is desirable to heat the **phase-change material** layer 24 to induce changes of the **phase-change material** layer 24 between the amorphous and crystalline states.

Detailed Description Text - DETX (6):

The interfacial layer 20 does not increase its conductivity with increasing temperature to the same degree as other available materials such as cobalt silicide. The reduced resistivity at increased temperature makes conventional materials less than ideal as heating electrodes for the **phase-change material** layer 24. At relatively high temperatures, such as 600.degree. C., where the resistivity of other materials decreases, the effectiveness of the interfacial layer 20 as a heater to induce phase changes is not substantially diminished.

Detailed Description Text - DETX (10):

In some embodiments of the present invention, a layer (not shown) may be provided to improve the adhesion between the **phase-change material** layer 24 and the carbon-containing interfacial layer 20. Suitable adhesion promoting layers may include any conductive materials including titanium, titanium nitride and Tungsten, as a few examples.

Detailed Description Text - DETX (14):

Turning to FIG. 7, in one embodiment, the **phase-change material** layer 24 may be formed into the pore 18 and specifically into the region defined by the sidewall spacer 22 so as to contact the layer 20. An upper electrode 26 may be deposited over the **phase-change material** 24. Then, the electrode 26 and the **phase-change material** 24 may be patterned and etched to form the structure shown in FIG. 1.

Detailed Description Text - DETX (15):

Through the use of a carbon-containing interfacial layer 20, the resistivity of the **phase-change material** heater may be substantially increased while at the same time improving the heating performance of the heater at high temperatures. The heater effectively includes the series combination of the lower electrode 14 and the carbon-containing interfacial layer 20. However, a series resistive combination is dominated by the element with the higher resistance, which may be the carbon-containing interfacial layer 20 in some embodiments. As a result, the resistance of the series combination of layers 20 and 14 may be dominated by the resistance of the interfacial layer 20.

Detailed Description Text - DETX (18):

The bus 54 may be coupled to a basic input/output system (BIOS) memory 62 and to a serial input/output (SIO) device 56. The device 56 may be coupled to a mouse 58 and a keyboard 60, for example. Of course, the architecture shown in FIG. 8 is only an example of a potential architecture that may include the memory 48 using the **phase-change material**.

Claims Text - CLTX (1):

1. A memory comprising: a surface; a silicon carbide interfacial layer over said surface; and a **phase-change material** over said silicon carbide layer.

Claims Text - CLTX (5):

5. The memory of claim 4 wherein said **phase-change material** is formed on said carbon-containing interfacial layer and in said pore.

Claims Text - CLTX (7):

7. The memory of claim 6 wherein said sidewall spacer is positioned between said interfacial layer and said **phase-change material**.

Claims Text - CLTX (8):

8. The memory of claim 1 wherein said **phase-change material** includes a chalcogenide material.

Claims Text - CLTX (9):
9. An electronic device comprising: digital signal processor; and a memory coupled to said processor, said memory including a surface, a silicon carbide interfacial layer over said surface and a **phase-change material** over said silicon carbide layer.

Claims Text - CLTX (13):
13. A memory comprising: a semiconductor substrate; a silicon carbide layer positioned over said substrate; and a **phase-change material** over said silicon carbide layer.

Claims Text - CLTX (15):
15. The memory of claim 14 including an insulator over said conductive layer, said insulator having a pore defined therein, and said **phase-change material** and said silicon carbide layer being formed in said pore.

Claims Text - CLTX (17):
17. The memory of claim 16 wherein said **phase-change material** includes chalcogenide.

Claims Text - CLTX (18):
18. The memory of claim 17 including a sidewall spacer between said **phase-change material** and said silicon carbide layer.